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IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An electronic circuit, comprising:

a plurality of input/output (I/O) nodes for connecting the electronic circuit to at least a further electronic circuit ~~via interconnects~~;

a test unit for testing the ~~interconnects~~ electronic circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of

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inputs of the combinatorial circuit; and

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit; and

~~characterized in that~~ the second selection of I/O nodes further comprises a second I/O node that is coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that ~~bypasses the combinatorial circuit~~ includes at least one of a buffer and an inverter.

2. (Currently amended) ~~An~~ The electronic circuit as claimed in claim 1, ~~characterized in that~~ wherein the second selection of I/O nodes further comprises a third I/O node being coupled to a further I/O node from the first selection of I/O nodes in the test mode via a further connection that bypasses the combinatorial circuit.

3. (Currently amended) An electronic circuit ~~as claimed in claim 2, characterized in that~~, comprising:

a plurality of input/output (I/O) nodes for connecting the

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electronic circuit to at least a further electronic circuit;

a test unit for testing the electronic circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit;

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit;

the second selection of I/O nodes further comprises a second I/O node that is coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that bypasses the combinatorial circuit; and

at least one of the second I/O node is coupled to the I/O node from the first selection of I/O nodes via a buffer circuit and the third I/O node is coupled to the further I/O node from the first

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selection of I/O nodes via an inverter.

4.(Currently amended) ~~An~~ The electronic circuit as claimed in claim 1, ~~characterized in that the electronic circuit comprises~~ further comprising a test control node, the electronic circuit being arranged to switch to the test mode responsive to the reception of a test control signal on the test control node.

5.(Currently amended) ~~An~~ The electronic circuit as claimed in claim 1, ~~characterized in that the electronic circuit comprises~~ further comprising a main unit being logically connected to the I/O nodes in a functional mode of the electronic circuit, the main unit being arranged to bring the electronic circuit into the test mode upon receipt of a test control signal in a form of a predefined bit pattern through at least a subset of the first selection of I/O nodes.

6.(Currently amended) An electronic circuit arrangement, comprising:

an electronic circuit as claimed in claim 4 or 5; and

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a further electronic circuit connected ~~to the electronic circuit having interconnects~~ with the further electronic circuit;

~~characterized in that~~ wherein the further electronic circuit is arranged to provide the electronic circuit with the test control signal and to provide the first selection of I/O nodes with test patterns for testing the ~~interconnects~~ electronic circuit.

7. (Currently amended) ~~An~~ The electronic circuit arrangement as claimed in claim 6, ~~characterized in that~~ wherein the further electronic circuit is arranged to receive test result data from the second selection of I/O nodes.

8. (Currently amended) A method for testing ~~interconnects between~~ an electronic circuit ~~and a further electronic circuit~~, the electronic circuit comprising:

a plurality of input/output (I/O) nodes for connecting the electronic circuit to ~~the~~ a further electronic circuit ~~via the interconnects~~;

a test unit for testing the ~~interconnects~~ electronic

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circuit in a test mode of the electronic circuit, the test unit comprising a combinatorial circuit having a plurality of inputs and an output, the combinatorial circuit implementing an exclusive logic function;

the I/O nodes being logically connected to the test unit in the test mode, wherein:

a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit; and

a second selection of the I/O nodes comprises a first I/O node and is arranged to carry respective output signals, the first I/O node being coupled to the output of the combinatorial circuit;

the method comprising the ~~steps~~ acts of:

logically connecting the test unit to the ~~interconnects~~ electronic circuit;

putting test data ~~on the interconnects~~ to the electronic circuit by the further electronic circuit; and

receiving test result data through the first I/O node;

~~characterized in that the method further comprises the step of~~

receiving further test result data through a second I/O

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node from the second selection of I/O nodes, the second I/O node being coupled to an I/O node from the first selection of I/O nodes in the test mode via a connection that ~~bypasses the combinatorial circuit~~ includes at least one of a buffer and an inverter.

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